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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,534	06/14/2001	Garo J. Derderian	MI22-1752	8714

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EXAMINER
THOMAS, TONIAE M

ART UNIT	PAPER NUMBER
2822	16

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,534	DERDERIAN ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- Th MAILING DATE of this communication appears on th cover sh t with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32,33,36,37,40,41,44-46 and 49-51* is/are rejected.

7)☒ Claim(s) *34,35,38,39,42,43,47 and 48* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is an official response to the amendment filed on 03 April 2003. Currently, claims 32-52 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. *Claims 32, 33, 36, 37, 40, 41, 44, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 6,218,260 B1) and Kim et al. (US 6,391,803 B1).*

Regarding claims 32, 33, 40, 41, 44, and 50

Lee et al. disclose a memory array (figs. 1A, 1B, and accompanying text). The memory array comprises: a plurality of capacitor constructions, each having a first capacitor electrode 21 over a substrate 2, a capacitor dielectric layer 23 over the first electrode, a second capacitor electrode 24 over the dielectric layer, and an insulative barrier layer 22 to oxygen diffusion between the first and second electrodes. The insulative barrier layer is a chemical vapor deposited (CVD) silicon nitride layer, which is formed between the first electrode 21 and the capacitor dielectric layer 23 (fig. 1B; col. 7, lines 12-17; and col. 9, line 33 – col. 10, line 29).[1] The first electrode 21 comprises conductive layer 21a and HSG layer 21b, and the capacitor dielectric layer 23

comprises a Ta_2O_3 layer (col. 4, lines 30-44). Lee et al. disclose a barrier layer having a thickness of less than about 12 Å (col. 10, lines 28-29).

Lee et al. do not teach that the silicon nitride barrier layer is an atomic layer deposited (ALD) silicon nitride layer. However, Kim et al. disclose a silicon nitride layer 8 (fig. 5). The silicon nitride layer 8 is an ALD silicon nitride layer (figs. 1-5 and col. 3, line 61 – col. 4, line 26). The silicon nitride layer comprises a chemisorption product of first and second substantially saturated precursor monolayers, wherein the precursors are different (fig. 5 and col. 3, line 61 – col. 4, line 25).

Kim et al. suggest using the ALD silicon nitride between a Ta_2O_5 dielectric layer and the first electrode of a capacitor (col. 3, lines 10-15). At the time the invention was made, one having ordinary skill in the art would have been motivated to modify Lee et al. by using an ALD silicon nitride layer between the first electrode 21 and the Ta_2O_3 dielectric layer 23 instead of the CVD silicon nitride layer, as taught by Kim et al., because an ALD silicon nitride layer has excellent step coverage when compared with a CVD silicon nitride layer. Since an ALD silicon nitride layer has excellent step coverage, it conforms to the uneven surface of the first electrode 21 caused by the HSG layer 21b much better than a CVD silicon nitride layer.

Regarding claims 36 and 37

Lee et al. disclose a capacitor (figs. 1A, 1B, and accompanying text). The capacitor comprises: a first capacitor electrode 21 over a substrate 2 (fig. 1B); an insulative barrier layer 22 to oxygen diffusion over the first electrode (fig. 1B); a

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[1] Silicon nitride is a well known insulative barrier to oxygen diffusion.

capacitor dielectric layer 23 over the first electrode (fig. 1B); and a second capacitor electrode 24 over the dielectric layer and the barrier layer (fig. 1B). As discussed above, the insulative barrier layer 22 is a CVD silicon nitride layer, which is formed between the first electrode 21 and the capacitor dielectric layer 23 (fig. 1B; col. 7, lines 12-17; and col. 9, line 33 – col. 10, line 29). Again, the first electrode 21 comprises conductive layer 21a and HSG layer 21b, and the capacitor dielectric layer 23 comprises a Ta_2O_3 layer (col. 4, lines 30-44). As discussed above, Lee et al. disclose a barrier layer having a thickness of less than about 12 Å (col. 10, lines 28-29).

Lee et al. do not teach that the silicon nitride barrier layer 22 comprises a chemisorption product of first and second precursor monolayers. As discussed above, Kim et al. disclose a silicon nitride layer 8 (fig. 5). The silicon nitride layer 8 is an ALD silicon nitride layer (figs. 1-5 and col. 3, line 61 – col. 4, line 26). The silicon nitride layer comprises a chemisorption product of first and second precursor monolayers, wherein the precursors are different (fig. 5 and col. 3, line 61 – col. 4, line 25).

Kim et al. suggest using the ALD silicon nitride layer between a Ta_2O_5 dielectric layer and the first electrode of a capacitor (col. 3, lines 10-15). At the time the invention was made, one having ordinary skill in the art would have been motivated to modify Lee et al. by using an ALD silicon nitride layer between the first electrode 21 and the Ta_2O_3 dielectric layer 23 instead of a CVD silicon nitride layer, as taught by Kim et al., because an ALD silicon nitride layer has excellent step coverage when compared with CVD a silicon nitride layer. Since an ALD silicon nitride layer has excellent step coverage, it

conforms to the uneven surface of the first electrode 21 caused by the HSG layer 21b much better than a CVD silicon nitride layer.

3. *Claims 45, 46, 49, and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. in view of Kim et al. as applied to claims 32, 33, 40, 41, 44, and 50 above, and further in view of Wolf et al. (Silicon Processing for the VLSI Era – Vol. 1: Process Technology).*

Lee et al. teach that the capacitors are formed on a p-type semiconductor substrate or wafer (col. 3, lines 59-63). One can infer from this that the p-type semiconductor substrate is p-type monocrystalline silicon. However, Lee et al. do not explicitly teach that the substrate is a monocrystalline (i.e. single-crystal) semiconductor. Wolf et al. show that the use of single-crystal silicon wafers is conventional and well known in the art (page 1, paragraphs 1-3). Therefore, the limitation "a monocrystalline semiconductor wafer" is obvious over the combination of Lee et al. and Kim et al.

Allowable Subject Matter

4. *Claims 34, 35, 38, 39, 42, 43, 47, and 48 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.* The prior art of record does not anticipate, teach, or suggest an insulative barrier layer to oxygen, the barrier layer comprising a chemisorption product of first and second precursor

monolayers, wherein the barrier layer comprises Al_2O_3, or wherein the barrier layer has a k factor greater than about 7.[2]

Response to Arguments

5. Applicant's arguments, filed 03 April 2003, with respect to the rejection of claims 36, 38, and 39 under 35 USC 102(e) and the rejection of claims 32-35, 37, and 40-51 under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejections have been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Lee et al. (US 6,218,260) and Kim et al. (US 6,391,803).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (703) 305-7646. The examiner can normally be reached on Monday through Thursday, and alternating Fridays, from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TMT
June 11, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

[2] "K factor" is interpreted to mean dielectric constant.